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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/605,982 | 11/12/2003 | Kai D. Feng | BUR920030142US1 | 2981 |

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SCHMEISER, OLSEN + WATTS
SUITE 201
3 LEAR JET
LATHAM, NY 12033

| EXAMINER | |
|---|---|
| NGUYEN, MINH T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 10/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/605,982 | FENG, KAI D. | |
| | Examiner | Art Unit | |
| | Minh Nguyen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-10 and 12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-10 and 12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Applicant's amendment filed on 9/7/04 has been received and entered. Claims 2-10 and 12-20 are pending. The amendment and argument presented therein overcome the informality objections and indefiniteness rejections, and therefore, are withdrawn. However, the prior art rejections are remained for the reasons set forth below. This action is FINAL.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2-5 and 12-15 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,646,563, issued to Kuo.

As per claim 2, Kuo discloses a PLL (Fig. 4), comprising:

a voltage controlled oscillator (VCO 440) for providing a first signal (VCO_IN);

a phase comparator (310) for comparing the first signal (VCO_IN) to a reference signal (REF_IN) and providing a control signal (CNTRL_N and CNTRL_P); and

a charge pump circuit (320) comprising a current source (340), a first FET (328), a second FET (326), a first capacitor (C1) wherein the first FET, second FET and first capacitor electrically coupled (as shown, they are electrically connected in the charge pump circuit 340),

wherein the current source is directly connected to the source of the first FET (as shown, the current source 340 is directly connected to VSS and the source of the first FET 328 is also directly connected to VSS), wherein the second FET comprises a parasitic capacitance (every FET has this element when the FET is operated in a switching environment), wherein the charge pump circuit is for receiving the control signal (CNTRL_N and CNTRL_P) and performing the recited function (any PLL performs the recited function), and wherein the second FET comprises parasitic capacitance that is to direct the spark current to ground (the frequency of noise, i.e., jitters or spark current are noise, caused by the switching action is much higher than the switching frequency, and therefore, parasitic capacitance exists between terminals of the second FET to ground, this parasitic capacitance acts as a filter to direct the jitters to ground), the charge pump circuit compensates for a spark current resulting from a switching mode of the control signal (column 4, lines 1-14, i.e., the structure of the charge pump 320 is for reducing the jitters (spark current) caused by the switching of the control signal).

As per claim 3, the first FET (328) clearly receives the control signal (CNTRL_N) at the gate, and since the first FET is an NFET, the functional recitation is met, i.e., ON at logic high and OFF at logic low.

As per claim 4, met since the recitation is merely the result of the operation.

As per claim 5, the first (328) and second (326) FETs are clearly NFETs.

As per claim 12, the claim is merely a method to operate a PLL having the structure noted in claim 2, since Kuo teaches the circuit, he inherently teaches the recited method.

As per claims 13-15, these claims are rejected for the same reasons noted in claims 3-5, respectively.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-10 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,646,563, issued to Kuo.

As per claim 6, Kuo discloses a PLL as discussed in claim 2 but he does not explicitly disclose the second FET is adjusted to operate in saturation mode as called for in the claim (actually, Kuo does not mention whether the first FET (326) is operated in saturation mode).

However, as ruled by the court, when a general condition is met, it is not inventive to modify the parameter to obtain the optimum result. In this instant case, Kuo teaches a PLL having the structure recited in claim 2 (general condition), the act of increasing and/or decreasing the current value of the current source (340) which resulting in driving the second FET (326) to saturation mode to obtain the optimum result is well within the level of one skilled in the art.

It would have been obvious to one skilled in the art at the time of the invention was made to adjust the current source (340) in the Kuo's PLL so that the second FET is operated in saturation mode for the motivation to obtain the optimum result is well within the level of one skilled in the art, i.e., by experiment, one skilled in the art can easily vary the value of the current source to find a value which will minimize the spark current using the structure taught by Kuo.

As per claim 7, the recited direct current voltage is the voltage at the gate of the second FET (326), and since the second FET is in saturation mode, the recited condition on the last three lines must be met.

As per claims 8-10, these claims are rejected for the same reasons and motivations as discussed in claim 6 herein above, i.e., Kuo explicitly discloses the structure as discussed in claim 2, it is not inventive to modify the parameters as recited in these claims to obtain the optimum conditions.

As per claims 16-20, these claims are rejected for the same reasons and motivation noted in claims 6-10, respectively.

### *Response to Arguments*

4. Applicant's argument filed on 9/7/04 has been fully considered but it is not persuasive. The argument is that Kuo does not teach or suggest the current source is directly connected to a source of a FET as called for in independent claims 2 and 11.

As discussed in the preceding rejection, in Fig. 4 of Kuo, he teaches the current source 340 is directly connected to VSS and the source of the first FET 328 is also directly connected to VSS. Therefore, the current source 340 is directly connected to the source of the first FET, the recited limitation is met.

### *Conclusion*

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10/8/04

Minh Nguyen
Primary Examiner
Art Unit 2816